Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A circuit comprising:

an interconnected plurality of semiconductor device structures arranged in an array characterized by a plurality of rows and a plurality of columns, each of said semiconductor device structures further comprising a gate electrode including a vertical sidewall and a gate dielectric disposed on the vertical sidewall, a plurality of semiconducting carbon nanotubes [[each]] extending substantially vertically between opposite respective first and second ends ~~at respective locations~~ adjacent to said vertical sidewall of said gate electrode, a first contact electrically coupled with said first end of each of said semiconducting carbon nanotubes, and a second contact electrically coupled with said second end of each of said semiconducting carbon nanotubes.

2. (Cancelled)

3. (Previously Presented) The circuit of claim 1 wherein each of said semiconducting carbon nanotubes is a single-wall semiconducting carbon nanotube.

4. (Cancelled)

5. (Previously Presented) The circuit of claim 1 wherein said first contact includes a catalyst pad characterized by a catalyst material effective for growing said semiconducting carbon nanotubes.

6. (Previously Presented) The circuit of claim 5 wherein said first end of said semiconducting carbon nanotubes incorporates an electrical-conductivity enhancing substance diffused from said catalyst pad into said first end during growth.

7. (Previously Presented) The circuit of claim 1 wherein each of said plurality of semiconductor device structures further comprises:

an insulating layer disposed between said first contact and said gate electrode for electrically isolating said first contact from said gate electrode.

8. (Previously Presented) The circuit of claim 1 wherein each of said semiconductor device structures further comprises:

an insulating layer disposed between said second contact and said gate electrode for electrically isolating said second contact from said gate electrode.

9. (Withdrawn) The circuit of claim 1 wherein each of said plurality of semiconductor device structures further comprises:

a third contact; and

at least one electrically-conducting carbon nanotube electrically coupling said gate electrode with said third contact.

10. (Withdrawn) The circuit of claim 1 wherein said second contact includes a vertically-extending metal post electrically coupled with said second end of said semiconducting carbon nanotubes.

11. (Withdrawn) The circuit of claim 10 wherein said second contact includes a conductive layer extending horizontally beneath said gate electrode for electrically coupling said catalyst pad with said metal post.

12. (Withdrawn) The circuit of claim 1 wherein said second contact includes at least one electrically conducting carbon nanotube extending substantially vertically and electrically coupled with said second end of each of said semiconducting carbon nanotubes.

13. (Withdrawn) The circuit of claim 12 wherein said second contact includes a conductive layer extending horizontally beneath said gate electrode for electrically coupling said second end of each of said semiconducting carbon nanotubes with said at least one electrically conducting carbon nanotube.

14. (Cancelled)

15. (Previously Presented) The circuit of claim 1 wherein said plurality of semiconductor device structures are interconnected as a memory circuit.

16. (Previously Presented) The circuit of claim 15 further comprising:

a plurality of word lines each electrically interconnecting said gate electrode of each of said plurality of semiconductor device structures located in a corresponding one of said plurality of rows of said array; and

a plurality of bit lines each electrically interconnecting said second contact of each of said plurality of semiconductor device structures located in a corresponding one of said plurality of columns of said array.

17. (Previously Presented) The circuit of claim 16 wherein each of said plurality of word lines comprises said gate electrode of each of said plurality of semiconductor device structures located in said corresponding one of said plurality of rows of said array.

18. (Previously Presented) The circuit of claim 16 wherein each of said plurality of bit lines comprises a conductive stripe electrically coupling said source of each of said plurality of

semiconductor device structures located in a corresponding one of said plurality of rows of said array.

19. (Previously Presented) The circuit of claim 1 further comprising:

a substrate carrying said plurality of semiconductor device structures and characterized by a surface area viewed vertical to the substrate, said plurality of semiconductor device structures separated by a space filled by a dielectric material, and said space ranging from about 20 percent to about 50 percent of said surface area.

20. (Withdrawn) The circuit of claim 1 wherein said plurality of semiconductor device structures are interconnected as a logic circuit.

21-33. (Cancelled)

34. (Previously Presented) The circuit of claim 5 wherein said catalyst pad further comprises nanocrystals of the catalyst material.

35. (Previously Presented) The circuit of claim 1 wherein each of said semiconductor device structures further comprises:

a capacitor electrically coupled with said first contact.

36. (Withdrawn) The circuit of claim 13 wherein each of said semiconductor device structures further comprises:

a catalyst pad electrically coupling said electrically conducting carbon nanotube with said conductive layer, said catalyst pad participating in the synthesis of said electrically conducting carbon nanotube.

37. (Withdrawn) The circuit of claim 36 wherein said catalyst pad further comprises nanocrystals of the catalyst material.

38. (Withdrawn) The circuit of claim 11 further comprising:

an insulating layer positioned between said conductive layer and said gate electrode, said insulating layer electrically isolating said gate electrode from said conductive layer.

39. (Withdrawn) The circuit of claim 11 further comprising:

a substrate carrying said plurality of semiconductor device structures, said conductive layer being arranged vertically between said gate electrode and said substrate.

40. (Withdrawn) The circuit of claim 13 further comprising:

an insulating layer positioned between said conductive layer and said gate electrode, said insulating layer electrically isolating said gate electrode from said conductive layer.

41. (Withdrawn) The circuit of claim 13 further comprising:

a substrate carrying said plurality of semiconductor device structures, said conductive layer being arranged vertically between said gate electrode and said substrate.

42. (Withdrawn) The circuit of claim 9 wherein each of said semiconductor device structures further comprises:

a catalyst pad electrically coupling said electrically conducting carbon nanotube with said gate electrode, said catalyst pad participating in the synthesis of said electrically conducting carbon nanotube.

43. (Currently Amended) A circuit comprising:

an interconnected plurality of semiconductor device structures, each of said plurality of semiconductor device structures further comprising a gate electrode including a vertical sidewall and a gate dielectric disposed on the vertical sidewall, a plurality of semiconducting carbon nanotubes [[each]] extending substantially vertically between opposite respective first and second ends ~~at respective locations~~ adjacent to said vertical sidewall of said gate electrode, a first

contact electrically coupled with said first end of each of said semiconducting carbon nanotubes, and a second contact electrically coupled with said second end of each of said semiconducting carbon nanotubes.

44. (Previously Presented) The circuit of claim 43 wherein each of said semiconducting carbon nanotubes is a single-wall semiconducting carbon nanotube.

45. (Cancelled)

46. (Previously Presented) The circuit of claim 43 wherein said first contact includes a catalyst pad characterized by a catalyst material effective for growing said semiconducting carbon nanotubes.

47. (Previously Presented) The circuit of claim 43 wherein each of said plurality of semiconductor device structures further comprises:

an insulating layer disposed between said first contact and said gate electrode for electrically isolating said first contact from said gate electrode.

48. (Previously Presented) The circuit of claim 43 wherein each of said plurality of semiconductor device structures further comprises:

an insulating layer disposed between said second contact and said gate electrode for electrically isolating said second contact from said gate electrode.

49. (Withdrawn) The circuit of claim 43 wherein each of said plurality of semiconductor device structures further comprises:

a third contact; and

at least one electrically conducting carbon nanotube electrically coupling said gate electrode with said third contact.

50. (Withdrawn) The circuit of claim 43 wherein said second contact includes a vertically-extending metal post electrically coupled with said second end of each of said semiconducting carbon nanotubes.

51. (Withdrawn) The circuit of claim 43 wherein said second contact includes at least one electrically conducting carbon nanotube extending substantially vertically and electrically coupled with said second end of each of said semiconducting carbon nanotubes.

52. (Previously Presented) The circuit of claim 43 further comprising:

a substrate carrying said plurality of semiconductor device structures and characterized by a surface area viewed vertical to the substrate, said plurality of semiconductor device structures separated by a space filled by a dielectric material, and said space ranging from about 20 percent to about 50 percent of said surface area.

53. (Previously Presented) The circuit of claim 43 wherein each of said semiconductor device structures further comprises:

a capacitor electrically coupled with said first contact.